Abstract

The invention provides a method for fabricating a semiconductor memory component, in particular a DRAM or FRAM, having a silicon substrate, an intermediate oxide layer (1) arranged on said substrate, an upper layer (3, made of a ferroelectric material or made of a material having a high dielectric constant being arranged on said intermediate oxide layer, a contact hole (8) extending as far as the interface between the silicon substrate and the upper layer being introduced by means of etching proceeding from an opening (5) in a perforated mask, which was formed in a preceding step. For the perforated mask, use is made of a material which is stable at high temperatures, to be precise stable at high temperatures so that O_3/TEOS-SiO_2 can subsequently be deposited onto this layer (e.g. polyimide) without degradation of this layer. The etching is performed using the perforated mask into the intermediate oxide layer (1) to form a depression (8'). A layer made of O_3/TEOS-SiO_2 is deposited onto the structure thus obtained. The layer made of O_3/TEOS-SiO_2 is removed from the bottom of the depression (8') by etching, and the depression (8') is thereupon lowered by etching in order to produce the contact hole as far as the interface with the silicon substrate, the latter being uncovered.

(Figure 2G)